

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

REJECTION CIRCUITRY FOR VARIABLE-GAIN AMPLIFIERS AND CONTINUOUS-TIME FILTERS

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**REJECTION CIRCUITRY FOR
VARIABLE-GAIN AMPLIFIERS AND CONTINUOUS-TIME FILTERS**

BACKGROUND OF THE INVENTION

5 **Field of the Invention**

The present invention relates to electrical signal processing, and, in particular, to circuitry that provides a variable-gain amplifier (VGA) function and/or a continuous-time filter (CTF) function.

Description of the Related Art

10 Fig. 1 shows a schematic circuit diagram of a prior-art MOSFET open-loop variable-gain amplifier (VGA) 100. VGA 100 has two equivalent, differential transistor pairs M6, M7 and M8, M9 connected, on the drain side, to two equivalent transconductance load devices M4 and M5 and, on the source side, to two current sinks 102 and 104. The differential input signal VIP, VIN is applied to the gates of the differential transistor pairs, while the differential output signal VOP, VON is presented at the drains of the differential transistor pairs. In particular, VIP is applied to the gates of M6 and M9, VIN is applied to the gates of M7 and M8, VOP is presented at a node shared by the drains of M7 and M9, and VON is presented at a node shared by the drains of M6 and M8.

15 Each transconductance load device is a MOSFET whose source is connected to the drain of one of the transistors in each differential pair and whose source and gate are both connected to reference voltage VDD. In particular, the source of M4 is connected to the drains of M6 and M8, while the source of M5 is connected to the drains of M7 and M9.

20 Each current sink is connected between the sources of both transistors in one of the differential pairs and reference voltage VSS (e.g., ground). In particular, current sink 102 is connected to a node shared by the sources of M6 and M7, while current sink 104 is connected to a node shared by the sources of M8 and M9. The current through current sink 104 is I_{neg} , while the current through current sink 102 is $I_{total}-I_{neg}$.

25 To achieve log-linear gain adjustment using VGA 100, the current I_{neg} is adjusted in a linear fashion (keeping I_{total} constant), providing near exponential gain control. A single pole ω_p at the output nodes is given by Equation (1) as follows:

$$30 \quad \omega_p = \frac{g_{mload}}{C_l} \quad (1)$$

where g_{mload} is the output transconductance due to the load devices, and C_l is the sum of all parasitic capacitances at the output node VON.

As indicated by Equation (1), the bandwidth of VGA 100 is limited by the output transconductance and load capacitance. In addition, common-mode and power-supply rejection are limited by the direct connection of the gain terminals of transconductors M4 and M5 to the power supply or voltage reference VDD.

SUMMARY OF THE INVENTION

Problems in the prior art are addressed in accordance with the principles of the present invention by a variable-gain amplifier that provides improved bandwidth, common-mode rejection, and power-supply rejection as compared with prior-art VGAs such as VGA 100 of Fig. 1, while maintaining log-linear gain control. In one embodiment, a triode-biased MOSFET device is added in series with the gate connection of the load devices, which creates complex poles at the VGA output.

In one embodiment, the present invention is circuitry comprising a first differential transistor pair (e.g., M6, M7) connected between a first load device (e.g., M4) and a first current sink (e.g., 102). A first inductance-creating element (e.g., M2) is connected to the first load device to add inductance at a first output node (e.g., VON) of the circuitry, and a power-supply rejection element (e.g., M1 and I1) is connected between the first inductance-creating element and a first voltage reference (e.g., VDD) to provide power-supply rejection at the first output node.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which like reference numerals identify similar or identical elements.

Fig. 1 shows a schematic circuit diagram of a prior-art MOSFET open-loop variable-gain amplifier;

Fig. 2 shows a schematic circuit diagram of a MOSFET open-loop variable-gain amplifier;

Fig. 3 shows a schematic circuit diagram of a circuit that implements a VGA, similar to the VGA of Fig. 2, and a continuous-time filter within a single set of circuitry; and

Fig. 4 shows a schematic circuit diagram of a continuous-time filter.

DETAILED DESCRIPTION

Reference herein to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment can be included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments necessarily mutually exclusive of other embodiments.

Fig. 2 shows a schematic circuit diagram of a MOSFET open-loop variable-gain amplifier 200. VGA 200 has all of the same components as prior-art VGA 100 of Fig. 1. In addition, VGA 200 has three MOSFET devices M1-M3, current source I1, common-mode sense circuit 206, and differential amplifier 207.

As shown in Fig. 2, instead of being directly connected to VDD as in Fig. 1, the gates of load devices M4 and M5 are connected to the drains of devices M2 and M3. The sources of devices M2 and M3 are both connected to the source of device M1, while the gates of M1-M3 and the drain of M1 are all connected to current source I1, whose other side is connected to VDD. Current sources I2 and I3 are connected between VDD and output nodes VOP and VON, respectively. As configured, devices M4 and M5 operate as source followers, devices M2 and M3 add resistance to the gates of M4 and M5, and device M1 is drain-connected like a diode.

Devices M2 and M3 create an inductive component to the output impedance of the load devices, where the equivalent inductance L is approximated by Equation (2) as follows:

$$20 \quad L \approx \frac{1}{g_{m4}z(1 - \frac{z}{p})}, \quad (2)$$

where g_{m4} is the output transconductance at output node VON due to device M4, z is given by Equation (3) as follows:

$$z = \frac{1}{R_{M2}(C_{gs} + C_{gd})}, \quad (3)$$

and p is given by Equation (4) as follows:

$$25 \quad p = \frac{g_{m4}}{C_{gs} + C_l + g_{m4}R_{M2}C_{gd}}, \quad (4)$$

where R_{M2} is the drain-to-source resistance of device M2 biased in triode mode (i.e., where the voltage from the drain to the source is proportional to the drain current, such that the device looks like a resistor), C_{gs} is the gate-to-source capacitance of M4, C_{gd} is the gate-to-drain capacitance of M4, and C_l is the sum of the parasitic capacitances at output node VON. See W.Z. Chen and C.H. Lu, "A 2.5 Gbps CMOS Optical Receiver Analog Front-End," IEEE 2002 Custom Integrated Circuits Conferences, pp. 359-362, June 2002, the teachings of which are incorporated herein by reference.

Devices M2 and M3 are biased by gate-drain connected device M1, yielding a drain-to-source resistance from M2 and M3 that is proportional to the transconductance of M1. The effect of the added series resistance is to create a pair of complex poles at the output nodes VOP, VON. Without this series resistance, only a single sigma-axis pole would be present. By adjusting the drain-to-source resistance of M2 and M3, the Q of the complex poles can be adjusted to achieve critical damping, thereby improving the rise time and bandwidth of the circuit.

Because the gates of load devices M4 and M5 are not connected directly to the power supply VDD (as in the prior art of Fig. 1), power-supply rejection (i.e., the inhibition of noise in power supply VDD from reaching the output nodes VOP, VON) is greatly improved.

Common-mode sense circuit 206 is connected to the output nodes VOP and VON to determine and track the common-mode voltage (i.e., the average of VOP and VON). The sensed common-mode voltage 208 is applied as a feedback signal to differential amplifier 207, which also receives a desired common-mode voltage Vcmref. Differential amplifier 207 generates and injects a correction signal at the sources of devices M1, M2, and M3 to compensate for errors between the sensed and the desired common-mode voltages. As such, differential amplifier 207 functions as a common-mode error amplifier that can provide considerable improvement in common-mode rejection (i.e., ensuring that the common-mode output voltage remains constant with changes in the common-mode input voltage).

Replica biasing (i.e., generating a bias for the circuit based on a piece of the circuit in order to compensate for temperature and/or process variations) can be used to improve the voltage headroom of the circuit. This can be particularly important in low-voltage applications, where additional headroom is beneficial.

Fig. 3 shows a schematic circuit diagram of a circuit 300, which implements a VGA, similar to VGA 200 of Fig. 2, and a continuous-time filter (CTF) within a single set of (e.g., integrated) circuitry. Combined VGA/CTF 300 has all of the same elements as VGA 200 of Fig. 2. In addition, circuit 300 has a pair of variable capacitors CL1-2 connected between reference voltage VSS (e.g., ground) and the output nodes VOP and VON, respectively. In addition, circuit 300 applies a control signal 310 to control

the current generated by current source I1, e.g., adjusting the magnitude of the current to control the equivalent resistance from devices M2 and M3.

Capacitors CL1-2 and control signal 310 add a low-pass filter (LPF) function to the VGA function provided by the amplifier circuitry of Fig. 2. Prior-art implementations for analog front end (AFE) circuitry requiring both variable-gain and continuous-time filtering involve separate stages: one for the VGA followed by one for the CTF. In order to provide a predictable bandwidth for the overall AFE, the VGA in these prior-art implementations has bandwidth in excess of the CTF cutoff frequency. By implementing the VGA and the CTF in a single (e.g., integrated) amplifier stage, combined VGA/CTF 300 greatly decreases power dissipation as compared to the prior-art implementation, by eliminating the need for excess bandwidth in a separate VGA stage and possibly decreasing the total number of amplifier stages.

In operation, MOSFET devices M2 and M3 are biased in triode mode and have an output resistance that is inversely proportional to the transconductance of device M1. As described previously in the context of Fig. 2, the addition of a controllable resistance in series with the gates of load devices M4 and M5 creates a complex output impedance. When combined with load capacitors CL1-2 and with parasitic capacitances from the other devices connected to the outputs, a pair of complex poles are created.

Assuming that (1) the capacitance C_L of capacitors CL1-2 is much greater than both the gate-to-drain capacitance C_{gdM4} and the gate-to-source capacitance C_{gsM4} of device M4 and (2) the sum of the output capacitances of all devices connected to the circuit outputs is relatively small, the output voltage V_{out} can be represented according to Equation (5) as follows:

$$V_{out} = V_{in} \frac{g_{mvga}}{C_L} * \left[\frac{1}{s^2 + \frac{s}{R_{M2}(C_{gdM4} + C_{gsM4})} + \frac{g_{M4}}{R_{M2}C_L(C_{gdM4} + C_{gsM4})}} \right], \quad (5)$$

where V_{in} is the input voltage, R_{M2} is the on-resistance of device M2 (or M3), g_{M4} is the transconductance of device M4 (or M5), and $g_{mvga} = g_{mpos} - g_{mneg}$, where g_{mpos} and g_{mneg} are the transconductances of the differential pairs M6, M7 and M8, M9, respectively.

The high-frequency response has a high-frequency parasitic pole and a complex pole pair with characteristics given by Equations (6) and (7) as follows:

$$\omega_o = \sqrt{\frac{g_{M4}}{R_{M2}C_L(C_{gdM4} + C_{gsM4})}} \quad (6)$$

$$Q = \sqrt{\frac{g_{M4}R_{M2}(C_{gdM4} + C_{gsM4})}{C_L}} \quad (7)$$

5 where both the cut-off frequency ω_o and Q are adjustable through R_{M2} and C_L . The low-frequency gain A_{LF} is adjustable according to Equation (8) as follows:

$$A_{LF} = \frac{g_{mvga}}{g_{M4}} \quad (8)$$

As the current I_{neg} is increased, the tail current ($I_{total}-I_{neg}$) for differential pair M6, M7 is decreased, yielding an approximately exponential gain dependency on I_{neg} . However, the total current 10 I_{total} for both differential pairs is constant with changes in I_{neg} . This keeps the transconductance g_{M4} constant, allowing both ω_o and Q to remain constant with gain adjustment. Higher-order filter functions and increased gain range can be achieved by cascading multiple instances of similar combined VGA/CTF stages.

15 Control signal 310 modulates current source I1, which in turn varies the transconductance of M1. The triode resistance R_{M2} of M2 and M3 is proportional to $1/g_{M1}$, where g_{M1} is the transconductance of M1. Since (1) R_{M2} is proportional to $1/g_{M1}$, (2) g_{M1} is proportional to the square root of I1, and (3) the Q is proportional to the square root of R_{M2} , the Q can be controlled by appropriately adjusting control signal 310. By the same token, since the cutoff frequency is proportional to $1/\sqrt{R_{M2}}$, control signal 310 also 20 adjusts the cutoff frequency.

Fig. 4 shows a schematic block diagram of a continuous-time filter 400. CTF 400 is similar to combined VGA/CTF circuit 300 of Fig. 3 without the second differential pair M8, M9. As such, CTF 400 provides the filter function of circuit 300 without providing the VGA function of circuit 300. One

significant advantage of this filter architecture is that a second-order filter section (i.e., a filter section having a pair of complex poles) can be created using a single amplifier.

Although the present invention has been shown as being implemented using particular MOSFET devices, those skilled in the art will understand that the present invention can be implemented using other types of devices. For example, p devices can be implemented using n devices, and vice versa. In 5 addition, one or more or all of the devices could be implemented using a different IC technology such as bipolar technology.

The present invention may be implemented as circuit-based processes, including possible implementation as a single integrated circuit (such as an ASIC or an FPGA), a multi-chip module, a 10 single card, or a multi-card circuit pack.

It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the scope of the invention as expressed in the following claims.

15 The use of figure numbers and/or figure reference labels in the claims is intended to identify one or more possible embodiments of the claimed subject matter in order to facilitate the interpretation of the claims. Such use is not to be construed as necessarily limiting the scope of those claims to the embodiments shown in the corresponding figures.